REFERENCE WAFER AND PROCESS FOR MANUFACTURING SAME

REFERENCE TO PRIORITY DOCUMENT

This Application claims priority to pending U.S. provisional application serial No. 60/254,271 filed December 8, 2000, and U.S. patent application serial No. 09/835,201 filed April 13, 2001, both applications entitled "Method And Apparatus For Self-Referenced Projection Lens Distortion Mapping", by Adlai Smith, Bruce McArthur, and Robert Hunter; U.S. provisional application serial No. 60/254,413 filed December 8, 2000 and U.S. patent application serial No. 09/891,699 filed June 26, 2001, both applications entitled "Method And Apparatus For Self-Referenced Wafer Stage Positional Error", to Adlai Smith, Bruce McArthur, and Robert Hunter; and U.S. provisional application serial No. 60/254,315 filed December 8, 2000 entitled "Reference Wafer and Process for Manufacturing Same", to Adlai Smith, Bruce McArthur, and Robert Hunter, all of which are incorporated by reference in their entirety herein.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to processes for semiconductor manufacture and more particularly to semiconductor pattern overlay.

2. Description of Related Art

Lithographic processing is increasingly requiring ever tighter layer-to-layer overlay tolerances to meet device performance requirements. Overlay registration on critical layers can directly impact device performance, yield and repeatability. Increasing device densities, decreasing device feature sizes and greater overall device size conspire to make pattern overlay one of the most important performance issues during the semiconductor manufacturing process. The ability to accurately determine correctable and uncorrectable pattern placement error depends on fundamental techniques and algorithms used to calculate lens distortion, stage error, and reticle error.

Overlay registration generally refers to translational error that exists between features exposed layer to layer in a vertical fabrication process of semiconductor devices on silicon wafers. Other names for overlay registration include, registration error and pattern placement error. A typical microelectronic device or circuit may consist of 20-30 levels or pattern layers. The placement of patterned features on other levels must match the placement of corresponding features on other levels, commonly referred to as overlap, within an accuracy which is some fraction of the minimum feature size or critical dimension (CD).

Overlay error is typically, although not exclusively, measured with an optical overlay metrology tool. *See* Semiconductor Pattern Overlay, N. Sullivan, SPIE Vol. 3051, 426:432, 1997; Accuracy of Overlay Measurements: Tool and Mark Asymmetry Effects, A. Starikov et al., Optical Engineering, 1298:1309, 1992; KLA 5105 Overlay Brochure, KLA-Tencor; KLA 5200 Overlay Brochure, KLA Tencor; Quaestor Q7 Brochures, Bio-rad Semiconductor Systems. Lithographers have crafted a variety of analysis techniques that attempt to separate out systematic process induced overlay error from random process induced error using a variety of statistical methods. *See* A Computer Aided Engineering Workstation for Registration Control, E. McFadden, C. Ausschnitt, SPIE Vol. 1087, 255:266, 1989; A "Golden Standard" Wafer Design for Optical Stepper Characterization, K. Kenp, C. King, W. W, C. Stager, SPIE Vol. 1464, 260:266, 1991; Matching Performance for Multiple Wafer Steppers using an Advanced Metrology Procedure, M. Van den Brink et al., SPIE Vol. 921, 180:197, 1988; Characterizing Overlay Registration of Concentric 5X and 1X Stepper Exposure Fields Using Interfield Data, F. Goodwin, J. Pellegrini, SPIE Vol. 3050, 407:417, 1997; Super Sparse Overlay Sampling Plans: An Evaluation of Methods and Algorithms for Optimizing Overlay Quality Control and Metrology Tool Throughput, J. Pellegrini, SPIE Vol. 3677, 72:82, 36220.

The importance of overlay error and its impact to yield can be found elsewhere. *See* Measuring Fab Overlay Programs, R. Martin, X. Chen, I. Goldberger, SPIE Conference on Metrology, Inspection, and Process Control for Microlithography XIII, 64:71, March 1999; A New Approach to Correlating Overlay and Yield, M. Preil, J. McCormack, SPIE Conference on Metrology, Inspection, and Process Control for Microlithography XIII, 208:216, March 1999. Lithographers have created statistical computer algorithms (for

example, Klass II (*See* Lens Matching and Distortion Testing in a Multi-Stepper, Sub-Micron Environment, A. Yost et al., SPIE Vol. 1087, 233:244, 1989) and Monolith (*See* A Computer Aided Engineering Workstation for Registration Control, *supra*)) that attempt to separate out correctable sources of pattern placement error from non-correctable sources of error. *See* Analysis of overlay distortion patterns, J. Armitage, J. Kirk, SPIE Vol. 921, 207:221, 1988; Method to Budget and Optimize Total Device Overlay, C. Progler et al., SPIE Vol. 3679, 193:207, 1999; and System and Method for Optimizing the Grid and Intrafield Registration of Wafer Patterns, J. Pellegrini, U.S. Patent 5,444,538 issued August 22, 1995. Overall theoretical reviews of overlay modeling can be found in *See* Semiconductor Pattern Overlay, *supra*; Machine Models and Registration, T. Zavecz, SPIE Critical Reviews Vol. CR52, 134:159.

Typically, most overlay measurements are made on silicon product wafers after each lithographic process, prior to final etch. Product wafers cannot be etched until the alignment attributes or overlay target patterns are properly aligned to the underlying overlay target patterns. Examples of overlay targets are described in Overlay Alignment Measurement of Wafers, N. Bareket, U.S. Patent 6,079,256 issued June 27, 2000 (at Fig 1b), Matching Management of Multiple Wafer Steppers Using a Stable standard and a Matching Simulator, M. Van den Brink et al., SPIE Vol. 1087, 218:232, 1989; Automated Electrical Measurements of Registration Errors in Step and Repeat Optical Lithography Systems, T. Hasan et al., IEEE Transactions on Electron Devices, Vol. ED-27, No. 12, 2304:2312, December 1980; Method of Measuring Bias and Edge Overlay Error for Sub 0.5 Micron Ground Rules, C. Ausschnitt et al., U.S. Patent 5,757,507 issued May 26, 1998; Capacitor Circuit Structure for Determining Overlay Error, K. Tzeng et al., U.S. Patent 6,143,621 issued November 7, 2000.

Generally, manufacturing facilities rely heavily on exposure tool alignment, wafer stage matching and calibration procedures (*See* Stepper Matching for Optimum Line Performance, T. Dooly, Y. Yang, SPIE Vol. 3051, 426:432, 1997; Matching Management of Multiple Wafer Steppers Using a Stable standard and a Matching Simulator, *supra*), Matching Performance for Multiple Wafer Steppers using and Advanced Metrology Procedure, *supra*) to help insure that the stepper or scanner tools are aligning properly;

inaccurate overlay modeling algorithms can corrupt the exposure tool calibration procedures and degrade the alignment accuracy of the exposure tool system. *See* Characterizing Overlay Registration of Concentric 5X and 1X Stepper Exposure Fields Using Interfield Data, *supra*.

Over the past 30 years the microelectronics industry has experienced dramatic, and rapid decreases in critical dimension in part due to improving lithographic imaging systems. *See* A New Lens for Submicron Lithography and its Consequences for Wafer Stepper Design, J. Biesterbos et al., SPIE Vol. 633, Optical Microlithography V, 34:43, 1986; New 0.54 Aperture I-Line Wafer Stepper with Field by Field Leveling Combined with Global Alignment, M. Van den Brink, B. Katz, S. Wittekoek, SPIE Vol. 1463, 709:724; Step and Scan and Step and Repeat, a Technology Comparison, M. Van den Brink et al., SPIE Vol. 2726, 734:753; 0.7 NA DUV Step and Scan System for 150nm Imaging with Improved Overlay, J. V. School, SPIE Vol. 3679, 448:463, 1999. Today, these photolithographic exposure tools or machines are pushed to their performance limits. As the critical dimensions of semiconductor devices approach 50nm the overlay error requirements will soon approach atomic dimensions. *See* Life Beyond Mix-and-Match: Controlling Sub-0.18 Micron Overlay Errors, T. Zavecz, Semiconductor International, July 2000. To meet the needs of next generation device specifications new overlay methodologies need to be developed. In particular, overlay methodologies that can accurately separate out systematic and random effects and break them into assignable causes may greatly improve device process yields. *See* A New Approach to Correlating Overlay and Yield, *supra*; Expanding Capabilities in Existing Fabs with Lithography Tool-Matching, F. Goodwin et al., Solid State Technology, 97:106, June 2000; Super Sparse Overlay Sampling Plans: An Evaluation of Methods and Algorithms for Optimizing Overlay Quality Control and Metrology Tool Throughput, *supra*; Lens Matching and Distortion Testing in a Multi-Stepper, Sub-Micron Environment, *supra*.

New "mix and match" technologies that can quickly and accurately reduce the registration error through better calibration and cross referencing procedures are desirable. *See* Mix-and-Match: A Necessary Choice, R. DeJule, Semiconductor International, 66:76, Feb 2000.

SUMMARY OF THE INVENTION

In accordance with the invention, a process for manufacturing, using, and maintaining a calibrated registration reference wafer for use in semiconductor manufacturing facilities is described. A reference reticle consisting of, for example, a 2-dimensional array of standard alignment attributes is exposed in an interlocking field pattern onto a photoresist coated semiconductor wafer using a photolithographic exposure tool. Following the lithographic development process, the resist patterned wafer is physically etched using standard techniques, thereby creating a permanent record of the alignment attribute exposure pattern. Along the interlocking rows and columns of the resulting wafer, the permanently recorded alignment attributes are measured for placement error using a conventional overlay metrology tool. The resulting overlay error data may be used, for example, in a software program, to generate a unique reference wafer calibration file that contains the positions of all the reference marks (alignment attributes) forming an uninterrupted, regular array across the wafer as well as the wafer alignment marks. The positions of these alignment attributes on the reference wafer can be determined very accurately, except for the possibility of arbitrary translation, rotation, asymmetric scaling and non-orthogonal positional offset errors.

The reference wafer and its associated calibration file can be used to determine the wafer stage registration performance for any photolithographic exposure tool. The accuracy and the precision of the calculated registration error are controlled, in large part, by the number of alignment attributes and overlay measurements. In addition, the process can be quickly repeated resulting in multiple reference wafers. Because of the ease of manufacture of this article, each photolithographic exposure tool in a semiconductor factory can have its own unique reference wafer for routine monitoring. Furthermore, the method of calculating the positional coordinates of the alignment attributes for the preferred reference wafer are more accurate and precise as compared to other techniques. The reference wafer, and its associated calibration file, may then be used as a calibrated ruler for measuring registration error induced by any photolithographic exposure tool, independently from a reference machine. Because a conventional overlay metrology tool is used for local measurements to extract global wafer stage and lens distortion, the above described process can be easily

implemented in a semiconductor fabrication facility. Additional applications of the resulting calibrated reference wafers include; improved lithographic simulation using conventional optical modeling software, advanced process control in the form of feedback loops that automatically adjust the projection lens, reticle stage, and wafer stage for optimum registration performance.

The reference wafer, or archive wafer, and its associated calibration file functions as a "ruler" and it can be used like a traditional "golden wafer" in the sense that an exposure of the reference marks 3302 illustrated in Figure 33, by any lithographic projection tool. For example, a set of complementary marks like the outer box 2702, illustrated in Figures 27 and 28 or the outer box 1302 and inner box 1304 marks illustrated in Figures 13A and 13B, result in a box-in-box structure or complete alignment attribute that can be measured with a conventional overlay metrology tool. Using the measurements from the overlay metrology tool and subtracting the corrections provided by the reference wafer calibration file from the overlay measurements, the combination of the intra-field and the inter-field errors of a machine can be directly interpreted. By accounting for stage distortion and yaw effects during the determination of the calibration, the inherent machine-to-machine reference errors of the prior art golden wafer method are effectively eliminated. *See* A "Golden Standard" Wafer Design for Optical Stepper Characterization, *supra*; Matching Management of Multiple Wafer Steppers Using a Stable standard and a Matching Simulator, *supra*.

Improvement in the measurement accuracy reduces the need for cross calibration between different photolithographic exposure tool sets and allows direct interpretation, after calibration file correction, of the results of a set of overlay measurements using the reference wafer. Errors in the overlay measurements due to the exposure of the present machine and not as due to systematic or random errors associated with the machine on which the reference wafer was manufactured. The technique described above can adjust the accuracy by adjusting the number of alignment attributes or overlay measurements.

A technique in accordance with the present invention includes providing a reticle, exposing a reference wafer in such a way as to create a unique pattern of overlapped interlocking alignment attributes, etching the reference wafer, measuring the interlocked alignment attributes, and finally creating a reference wafer calibration file that permanently

records the positional coordinates of the alignment attributes. Additionally, other embodiments may allow production of a robust set of reference wafers for manufacturing facilities that use scanners in addition to steppers. For this case, we minimize the non-repeatable source of intra-field error associated with the moving scanner stage during the exposure of the reference wafer by using a special reticle and multiple exposures. By utilizing a high precision overlay metrology tool for local measurements and extracting a global set of calibrated positional measurement, the metrology error multiplier can be kept near unity.

Figure 6 is a flow chart illustrating an embodiment for creating a reference wafer. In block 602, a reference reticle, for example the reticle illustrated in Figures 13A, 13B, 13C, 14 containing an array of alignment attributes 1302, 1304, 1306 and wafer alignment marks 1308, is loaded into an exposure tools' reticle management system 1002, as illustrated in Figure 10, and aligned. Wafers possibly laser or otherwise scribed with unique wafer identification codes and possibly coated with various thin films are provided. Examples of such thin films on silicon wafers are silicon nitride, silicon dioxide, amorphous silicon, or polysilicon.

Flow continues to block 604 where the wafer is then coated with photoresist and loaded into a projection imaging tool or machine and exposed, in block 606, in an overlapping interlocking pattern. Examples of overlapping interlocking patterns are illustrated in Figures 12 and 16A. The projection imaging tool may include contact or proximity printers, steppers, scanners, direct write, e-beam, x-ray, SCALPEL, IPL, or EUV machines. *See* Direct-Referencing Automatic Two-Points Reticle-to-Wafer Alignment Using a Projection Column Servo System, M. Van den Brink, H. Linders, S. Wittekoek, SPIE Vol. 633, Optical Microlithography V, 60:71, 1986; New 0.54 Aperture I-Line Wafer Stepper with Field by Field Leveling Combined with Global Alignment, *supra*; Refs 4861146, Micrascan™ III Performance of a Third Generation, Catadioptric Step and Scan Lithographic Tool, D. Cote et al., SPIE Vol. 3051, 806:816, 1997; Step and Scan Exposure System for 0.15 Micron and 0.13 Micron Technology Node, J. Mulkens et al., SPIE Conference on Optical Microlithography XII, 506:521, March 1999; 0.7 NA DUV Step and Scan System for 150nm Imaging with Improved Overlay, *supra*; Optical Lithography – Thirty Years and

Three Orders of Magnitude, J. Bruning, SPIE Vol. 3051, 14:27, 1997; Large Area Fine Line Patterning by Scanning Projection Lithography, H. Muller et al., MCM 1994 Proceedings, 100:104; Large-Area, High-Throughput, High-Resolution Projection Imaging System, K. Jain, U.S. Patent 5,285,236 issued February 8, 1994; Development of XUV Projection Lithography at 60-80 nm, B. Newnam et al., SPIE Vol. 1671, 419:436, 1992; Mix-and-Match: A Necessary Choice, *supra*. In the examples illustrated in Figures 12 and 16A, each exposure field is separated from the previous exposure by a desired distance such that neighboring fields have their corresponding interlocking rows or columns overlapped. *See* Mix-and-Match: A Necessary Choice, *supra*. This partially overlapping exposure technique is shown in Figures 12 and 16A. Following the exposures of the interlocking array, the wafer alignment marks and their corresponding interlocking rows and columns are exposed as separate fields but interlock into the previous exposure set.

Flow then continues to block 608 where, after the final exposure the wafer is removed from the machine and sent through the final few resist development steps. Next, the wafers are etched and stripped of photoresist and possibly overcoated with another layer. This leaves the alignment attributes and wafer alignment marks permanently recorded on the wafer surfaces. Flow then continues to block 610 where the resulting alignment attributes along the interlocking rows and columns are measured for registration, placement or overlay error using an overlay metrology tool such as a KLA-Tencor model 5200. *See* KLA 5200 Overlay Brochure, *supra*; KLA 5105 Overlay Brochure, *supra*; Quaestor Q7 Brochures, *supra*; Process for Measuring Overlay Misregistration During Semiconductor Wafer Fabrication, I. Mazor et al., U.S. Patent 5,438,413 issued August 1, 1995; Overlay Alignment Measurement of Wafers, *supra*. Figure 9 is a schematic illustrating common causes of overlay or placement error for inter-field and intra-field.

Next, in block 612, the intra-field distortion of the projection imaging tool used to create the reference wafer is provided. Flow continues to block 614 when the resulting data set is entered into a computer algorithm where a special calibration file containing the positional coordinates for each alignment attribute is constructed for the reference wafer. The final articles as created by the present invention consist of a reference wafer containing reference marks on a periodic array interrupted only by wafer alignment marks as illustrated

in Figure 33, and a unique calibration file that lists the location of each reference and wafer alignment mark on the wafer as illustrated in Figure 34. The process described above can be repeated multiple times resulting in numerous individual reference wafers. Once a calibration file is on record and the positions of each alignment attribute is known, the wafer can be used as a two dimensional (2-D) rigid ruler to measure the registration error associated with a given projection imaging tool - similar to the prior art golden wafer techniques. *See* A "Golden Standard" Wafer Design for Optical Stepper Characterization, *supra*. However, the preferred embodiment allows for the direct measurement of the overlay error unique to the machine being tested - without reference to another machine either directly or indirectly.

BRIEF DESCRIPTION OF THE DRAWINGS

The features of this invention believed to be novel and the elements characteristic of the invention are set forth with particularity in the appended claims. The figures are for illustration purposes only and are not drawn to scale. The invention itself, however, both as to organization and method of operation, may best be understood by reference to the detailed description which follows taken in conjunction the accompanying drawings in which:

Figure 1 is a schematic showing typical overlay patterns or completed alignment attributes.

Figure 2 is a schematic showing typical optical verniers.

Figure 3 is a schematic showing a reticle.

Figure 4 is a schematic showing overlapped male and female target pairs.

Figure5A is a schematic showing additional details of the reticle of Figure 3.

Figure 5B is a schematic showing additional details of Figure5A in developed positive photoresist.

Figure 6 is a flow chart of an embodiment for creating reference wafers.

Figure 7 is a flow chart of another embodiment for creating reference wafers.

Figure 8 is a flow chart illustrating an application of the reference wafer.

Figure 9 is a block diagram illustrating common causes of overlay or placement error.

Figure 10 is a block diagram showing a photolithographic stepper or scanner system.

Figure 11A is a schematic showing inter-field and intra-field overlay error.

Figure 11B is a schematic showing inter-field yaw error.

Figure 12 is a schematic showing additional detail of the interlocking of fields in X and Y directions on reference wafers.

Figure 13A is a schematic showing a reference reticle.

Figure 13B is a schematic showing a reference reticle that includes wafer alignment marks.

Figure 13C is a schematic showing exemplary inner and outer box sizes.

Figure 14 is a side view of a reference reticle.

Figure 15 is a schematic showing a further explanation of the components of the interlocking array of the reference reticle;

Figure 16A is a schematic showing a tiled or interlocking schematic of the reference wafer.

Figure 16B is a plan view showing an interlocking measurement site.

Figure 16C is a cross sectional view of an interlocking measurement site.

Figure 17A is a schematic showing typical overlapping regions showing 3 box in box overlay targets.

Figure 17B is a schematic showing examples of completed alignment attributes (box in box).

Figure 18 is a schematic showing an overlay error vector plot.

Figure 19 is a schematic showing a translation overlay vector plot.

Figure 20 is a schematic showing a rotation overlay vector plot.

Figure 21 is a schematic showing overlay measurement notation.

Figure 22 is a schematic showing an example of a golden wafer.

Figure 23 is a schematic showing a wafer alignment mark reticle.

Figure 24 is a schematic showing an inner box reticle.

Figure 25 is a schematic showing an example of a golden wafer layout.

Figure 26 is cross sectional view of an inner box.

Figure 27 is a schematic showing an outer box reticle.

Figure 28 is a schematic showing additional detail of an outer box reticle.

Figure 29 is a schematic showing an example of a golden wafer for overlay measurement.

Figure 30 is a cross section of a box in box.

Figure 31 is a schematic showing inter-field and intra-field indices.

Figure 32 is a schematic showing a partially exposed field.

Figure 33 is a schematic showing the operational portions of a completed reference wafer.

Figure 34 is a block diagram showing an exemplary calibration file for a reference wafer.

Figures 35A-35F are cross sectional views of a reference wafer.

Figure 36 is a schematic showing a reference wafer containing wafer alignment marks only.

DETAILED DESCRIPTION

The effects of overlay error are typically divided into two major categories for the purpose of quantifying overlay error and making precise exposure adjustments to correct the problem. The first category, referred to as grid or inter-field error, is the positional shift and rotation 1110 as illustrated in Figure 11A, or yaw 115 as illustrated in Figure 11B, of each exposure pattern, exposure field, or simply field, with reference to the nominal center position of the wafer. These global or inter-field positional errors may be caused by the wafer stage subsystem of the photolithographic exposure tool. Overlay modeling algorithms typically divide grid or inter-field error into various sub-categories or components the most common of which are translation, rotation, magnification or scale, non-orthogonality, stage distortion and stage rotation. *See* Matching Performance for Multiple Wafer Steppers using and Advanced Metrology Procedure, *supra*.

The second category, intra-field overlay error is the positional offset of an individual point inside an exposure field referenced to the nominal center of an individual exposure field 1120 in Figure 11A. Generally, the term "nominal center" means the location of the center of a perfectly aligned exposure field; operationally this is the (x,y) position where the

lithographic projection is commanded to print the exposure field (field). The following four components, each named for a particular effect, are typically used to describe the sources of intra-field error: translation, rotation, scale or magnification and lens distortion. Intra-field overlay errors are typically related to lens aberrations, reticle alignment, and dynamic stage errors for scanners. Separation of the overlay error into inter-field and intra-field components is based on the physically distinguishable sources of these errors, lens aberrations, dynamic stage errors, or reticle positioning for intra-field and the wafer stage for inter-field.

A process of creating and maintaining calibrated registration reference wafers that can be used to measure and determine the registration error associated with wafer stages and lenses of projection tools is described. The placement of patterned features on subsequent levels must match the placement of corresponding features on previous levels, i.e. overlap, within an accuracy which is typically some fraction of a minimum feature size or critical dimension (CD). Overlay registration is the localized translational error that exists between features exposed layer to layer in the vertical manufacturing process of semiconductor devices on silicon wafers. Overlay registration is also referred to as registration error or pattern placement error.

Inter-field error can be divided into various components of which the six most commonly used are: translation, rotation, scale, non-orthogonality, wafer stage distortion and stage yaw. *See* Matching Performance for Multiple Wafer Steppers using and Advanced Metrology Procedure, *supra*. In order to measure and quantify the overlay error that exists between device layers special overlay target patterns may be printed in designed locations across the wafer at each lithographic processing step. If the two patterned layers are perfectly aligned to each other the overlay target patterns will be aligned with each other. For example if a box-in-box target pattern were used, a centered box in box structure 2102 as illustrated in Figure 21 would result. Any positional offset or misalignment of the box-in-box target pattern 2104 is a measure of the overlay error, illustrated in Figure 21.

Figure 1 shows a variety of different overlay target patterns. There are many types of alignment attributes or overlay target patterns, for example, a box-in-box 102, a frame-in-frame 104, a segmented frame-in-frame 106, and a multi-segmented frame-in-frame 108 as

shown in Figure 1, optical verniers as shown in Figure 2, and gratings. The positional offset of these different target pattern is measured with a commercial optical overlay metrology tool. In some cases, the overlay error can be measured using the projection imaging tool's alignment system. *See* Matching Management of Multiple Wafer Steppers Using a Stable standard and a Matching Simulator, *supra*. Vector displacement plots as illustrated in Figures 18, 19 and 20, can be used to give a visual description of the direction and magnitude of overlay error are mathematically separated into different spatial components using a variety of regression routines. For example, an overlay plot 1802 illustrated in Figure 18 includes a translation component 1902, illustrated in Figure 19, plus a rotation component 2002, illustrated in Figure 20.

There are many commercial software packages that can be used to model and statistically determine the intra-field error components for the purpose of process control and exposure tool set-up. See, for example, (Monolith (*See* A Computer Aided Engineering Workstation for Registration Control, *supra*), Klass II (Lens Matching and Distortion Testing in a Multi-Stepper, Sub-Micron Environment, *supra*)). Once determined, the intra-field error components are analyzed and used to adjust calibration constants of the wafer handling stage to improve pattern alignment. In addition, because different exposure tools are used to produce a given device the exposure tools must be matched or fingerprinted and adjusted so that registration errors unique to one tool are removed or minimized as much as possible. *See* Mix-and-Match: A Necessary Choice, *supra*.

Golden Wafers

Finding the relative magnitude of wafer stage placement error, commonly uses a process of creating and using a "golden wafer". Using a golden wafer, the wafer stage placement error can be measured semi-independent of other sources of registration error. Semiconductor manufacturing facilities typically use the resulting placement error information to manually or automatically adjust the wafer stage and stepper alignment system in such a way so as to minimize the impact of overlay error. *See* Matching Management of Multiple Wafer Steppers Using a Stable standard and a Matching Simulator, *supra*; Matching Performance for Multiple Wafer Steppers using and Advanced Metrology Procedure, *supra*.

Figure 3 shows a typical set of geometrically placed overlay target patterns consisting of a matching pair of male 302 and female targets 304. The male 302 and female 304 targets may be regularly spaced across a wafer stage test reticle 306 as shown in Figure 3. Figures 5A and 5B show additional detail of the reticle shown in Figure 3.

It should be noted that typically the chrome target patterns on most reticles are 4 or 5 times larger as compared with the patterns they produce at the image plane, this simply means modem semiconductor projection imaging tools are reduction systems. Further, (by measuring the reticle and then applying these corrections) the overlay target patterns are placed in nearly perfect geometric positions on the wafer stage test reticle. For example, first, a photoresist coated wafer is loaded onto an exposure tool or stepper wafer stage and globally aligned. Next, the full-field image of the reticle is exposed several times at various positions across the surface of the photoresist coated wafer as illustrated in Figure 22. In addition, several wafer alignment marks 2202 may also be printed across the wafer using the reticle as illustrated in Figures 3 and 22. For example, the full-field of the reticle 306 may consist of an 11 by 11 array of male 302 and female 304 targets evenly spaced at pitch p' 308, across the reticle surface [Figures 3]. The pattern is then sent through the remaining portions of the lithographic patterning process to delineate the resist pattern. Finally, the patterned wafer is etched and the alignment attributes are permanently recorded in the wafer surface. This permanently etched wafer is called a golden wafer.

In general, the golden wafer may be used to extract stage errors on any photolithographic exposure tool in the following way. The golden wafer is loaded onto the wafer stage in question and aligned into position using the previously placed wafer alignment marks 2202 illustrated in Figure 22. Next, the wafer stage is moved so as to align the reticle 306 illustrated in Figure 3 containing, for example, an 11 by 11 array of male targets 302 directly on top of the first full-field exposure pattern containing an 11 by 11 array of female 304 targets resulting in overlapping targets 402 as illustrated in Figure 4 [Figures 4, 22]. Making these overlapping targets involves shifting the wafer the small increment d/M so male and female targets lie on top of one another. When the stepper has finished the alignment procedure the x,y wafer stage coordinates and overlay error associated with several male-female targets is electronically recorded. This step, align and record procedure

is repeated across a desired portion of the wafer for each full-field 11 by 11 exposure pattern. The electronically recorded target coordinates and overlay errors may then be entered into a statistical modeling algorithm to calculate the systematic and random components of inter-field and intra-field overlay error. It is important to note that the resulting inter-field or wafer stage overlay error not yield the unique overlay error of the wafer stage in question. Rather, it can only be used to report the inter-field or wafer stage overlay error as referenced to a golden wafer that was produced on another reference machine. In general, semiconductor manufacturers always rely on some kind of stage matching or cross-referencing technique to calculate the relative wafer stage overlay error.

There are several problems associated with the golden wafer technique. First, as noted above, the technique does not yield the unique wafer stage overlay error for the machine in question, it only provides a relative measure of all components. To obtain the relative stage error between two machines, the inter-field errors of each machine are determined and then subtracted from each other resulting in an increase in the noise in the stage error determination. Second, the models used to calculate the systematic inter-field error usually do not account for the stage error associated with distortion and yaw. These models are typically limited to translation, rotation, orthogonality and x and y scale errors (*See* A Computer Aided Engineering Workstation for Registration Control, *supra*), higher order errors are ignored or otherwise not taken into account. Relying on golden wafers created on a reference machine, results in wafers that are not identical, or have overlay deviations from one another even if they are exposed on a single machine in a short time to minimize machine instabilities. *See* Matching Management of Multiple Wafer Steppers Using a Stable standard and a Matching Simulator, *supra*. It would be very desirable to have an inter-field overlay technique that would can determine overlay error independently from a cross referenced golden wafer. *See* Mix-and-Match: A Necessary Choice, *supra*.

Reference Machine

Another technique utilizes a reference machine (projection imaging tool) for measurement of inter-field overlay error (*See* Matching Performance for Multiple Wafer Steppers using and Advanced Metrology Procedure, *supra*; Expanding Capabilities in Existing Fabs with Lithography Tool-Matching, *supra*). The reference machine is typically

one that is closest to the average of all machines in the factory (Expanding Capabilities in Existing Fabs with Lithography Tool-Matching, *supra*) or a machine that exhibits long term stability. *See* Matching Performance for Multiple Wafer Steppers using and Advanced Metrology Procedure, *supra*. On the reference machine, a golden wafer is exposed, developed and etched. The golden wafer is exposed using a desired target, for example, an inner box reticle 2402 as illustrated in Figure 24 that contains a regular array of inner box structures in a regular pattern covering the wafer, such as a 3 x 3 array 2502 as shown in Figure 25. Next, wafer alignment marks are exposed using a designated portion of the inner box reticle or a separate reticle containing the wafer alignment mark 2302 illustrated in Figure 23. The golden wafer is then typically etched and stripped to produce pits 2602 illustrated in Figure 26 corresponding to the inner box locations.

A number of such wafers may be produced and the locations of the inner box arrays (individual printings of the inner box reticle) then represent the inter-field positions of the reference machine. Next, a reticle containing outer box structures 2702 illustrated in Figures 27 and 28 in the same nominal positions as the inner box reticle (or the pattern required to produce a completed, machine readable alignment attribute (complementary pattern)), the outer box reticle, is placed on the machine to be measured, a completed golden wafer 2504 in Figure 25 is coated with photoresist, exposed and developed. The result is a developed golden or reference wafer 2902 illustrated in Figure 29, containing box in box structures that can then be measured on an overlay metrology tool. Figure 30 is a cross sectional view of a typical box-in-box structure shown in Figure 29.

The resulting measurements are then typically averaged over each field, for example, in Figure 29, the twenty-five measurements within each field would be averaged together to produce a net translation (Dxg, Dyg) and rotation (Yawg) for each of the nine fields. This averaged data is then fit to the following set of equations. *See* Matching of Multiple Wafer Steppers for 0.35 Micron Lithography using Advanced Optimization Schemes, M. van den Brink et al., SPIE Vol. 1926, 188:207, 1993; Matching Performance for Multiple Wafer Steppers using and Advanced Metrology Procedure, *supra*:

$$Dxg = Txg + sxg*xg + (-qg+qog)*yg + D2x*yg^2 + Rwx \qquad \text{(Eq 1)}$$

$$Dyg = Tyg + syg*yg + qg*yg + D2y*xg^2 + Rwy \quad \text{(Eq 2)}$$

$$Yawg = Qg + syawg*yg - 2*D2y*xg + Rwy \quad \text{(Eq 3)}$$

Where:

Dxg, Dyg, Yawg = x,y,yaw grid errors at grid position xg, yg

xg, yg= grid position = position on wafer with respect to the center of stage travel

Txg, Tyg = x,y grid translation

sxg, syg = x,y grid scale or magnification error

qg, qog= grid rotation, orthogonality

D2x, D2y = x,y stage bow terms

Rwx, Rwy, RwY = grid residual in the x, y, Yaw direction (we do not try fitting to these parameters).

The Yaw error (Yawg) is the deviation of the rotation of the projected field at a specific point. It results in a difference in field to field rotation as a function of placement position (xg, yg) on the wafer. The 10 unknown parameters (Txg, Tyg, ... D2x, D2y) in Equations 1, 2, 3 are solved for using least squares techniques. *See* Numerical Recipes, The Art of Scientific Computing, W. Press et al., Cambridge University Press, 509:520, 1990.

Problems with this technique include the systematic (repeatable) and random grid errors on the reference machine (the machine used for creating the golden wafers) are permanently recorded as half (inner or outer box) of our factory wide metrology standard. The magnitude and distribution of these errors is entirely unknown. For machine to machine comparisons of grid errors, the systematic part of the errors cancel out but the influence of the random or non-repeatable errors remains. To try and overcome this problem typically, multiple golden or reference wafers are used to improve machine to machine matching results. *See* Matching Management of Multiple Wafer Steppers Using a Stable standard and a Matching Simulator, *supra*. Furthermore, reference machine instabilities over time lead to a drift or error in the factory wide standard represented by the reference machine. Yet another problem with this technique is that because it utilizes full size projected fields to determine the inter-field errors, it does not work with partially exposed fields 3202 illustrated in Figure 32. The ability to include partially exposed fields is important because product

wafers typically contain multiple die within an exposure field and therefore the inter-field error of partially exposed fields directly affects the edge die overlay error.

Reference Reticles

Figure 13A shows a reference reticle 1310 containing an Nx+2 by Ny+2 array of overlay targets or box structures used for creating the basic interlocking array pattern on a substrate. The substrate may be different materials, for example, a silicon wafer, a quartz wafer, a flat panel display, a reticle, a photo-mask, or a mask plate, This reticle 1310 creates the basic periodic grid on a wafer with pitch P/M (M is the reduction magnification ratio of the projection imaging tool) and also creates the features that overlap or interlock from field to field and thereby improve accuracy. Figure 15 illustrates additional detail of the components of the interlocking array. In the middle is an Nx X Ny reference mark array 1502 on pitch P. These features become part of the wafer scale P/M grid and include a set of inner boxes 1304 as detailed in Figure 13A. On the right side of Figure 15 is the right interlocking column 1504. It consists of an Ny long set of outer boxes 1304 detailed in Figure 13A, at the indicated X and Y positions. The position of this column is determined so that the inner boxes in the left interlocking column 1506 of a subsequent exposure of the reticle, precisely overlap them on the wafer when the interlocking array is stepped and printed an X distance Sx=Nx*P/M at the wafer.

The left interlocking column 1506 includes an Ny long set of inner boxes that are off pitch (by the amount G) relative to the Nx X Ny reference mark array. The left interlocking column is off pitch (P-G spacing in Figure 13A), so that an array of reference marks uninterrupted by field boundaries can be created and also be able to create a system of interlocking columns 1202 as shown in Figure 12.

Figure 15 also details the position of the bottom 1508 and top 1510 interlocking rows, both of which contain Nx features. Their function and location is analogous to the function and position of the left 1506 and right 1504 interlocking columns respectively. The relative Y position of the top 1510 and bottom 1508 interlocking rows is determined to overlap the inner boxes of the bottom interlocking row when the projected field is stepped a distance Sy=Ny*P/M at the wafer.

In addition to the reference reticle of Figure 13A, another reference reticle containing wafer alignment marks is provided as illustrated in Figure 13B. The description and layout of this reticle is identical to the description above, the only difference is that where the wafer alignment mark of Figure 13B either covers a reference mark within the Nx X Ny reference array, or where the design rules for the wafer alignment mark dictate prescribed featureless areas, this reticle will contain no reference array marks. There will be a wafer alignment mark present or more typically several wafer alignment marks, one for each tool type used in the fab. The reticle containing the full interlocking array, Figure 13A, and any reticles with wafer alignment marks, Figure 13B, are then sequentially loaded and aligned on the projection imaging tool (machine) on which we will be manufacturing reference wafers.

Figure 13C illustrates some typical inner and outer box sizes, for use on an M=4 or 5 stepper or scanner while a typical reticle pitch P= 10mm and offset G=0.5mm. For these parameters Nx and Ny may be selected so that Nx=NY=8 thus allowing for the manufacture of reference wafers on either standard field steppers or scanners.

Wafers

As described above in block 604 of Figure 6, wafers are then provided. These wafers can be, for example, blank silicon or quartz (*See* Matching Management of Multiple Wafer Steppers Using a Stable standard and a Matching Simulator, *supra*) and may possibly laser scribed with an appropriate wafer id number for future identification 3304 as shown in Figure 33. If desired, the silicon reference wafers can be coated with a thin film of silicon nitride or silicon dioxide before continuing (quartz wafers would typically be chrome coated). Next, the wafer is coated with resist and loaded onto the wafer stage of the machine.

Interlocking Reference Mark Exposures

A series of exposures, each containing an Nx+2 by Ny+2 array of box structures, is made in an overlapping interlocking pattern. Figures 12 and 16A are examples of an interlocking pattern. Following the first exposure, subsequent exposures in the same row are separated by a distance of Sx=Nx*P/M or the distance between the leftmost inner box of the projected field and the rightmost outer box of the field. Subsequent exposures in the same column are separated by a distance of Sy=Ny*P/M or the distance between the inner box at the bottom of the projected field and the topmost outer box within the projected field. P is

the reticle pitch of reference marks within the Nx X Ny reference mark array as shown in Figure 15. M is the reduction magnification ratio of the machine. This field placement pattern creates an interlocking array of fields. Figure 12 shows additional detail of the interlocking array and Figure 16A shows a schematic of the entire resulting wafer.

An example of the final interlocking exposure pattern is shown in Figure 16A. It forms an Nfx X Nfy rectangular array of fields, the only missing fields being those allocated for wafer alignment marks or where a field position is not desired. Figure 16B is a plan view of an interlocking measurement site and Figure 16C is a cross sectional view of interlocking measurement sites of Figure 16B. Figure 17A is a diagram showing typical overlapping regions of three box-in-box overlay targets. Figure 17B illustrates a perfectly centered overlay target box measurement site and sign conventions for displacement.

The Nfx X Nfy array can contain partially exposed fields 3302 as shown in Figure 32, where the entire field is not printed on the wafer. These partial fields are important because the large exposure fields in modem steppers and scanners allow for multiple product die within a field (such as illustrated in Nikon Lithography Tool Brochures (Japanese), Nikon). Thus partially exposed fields 3202 can print multiple product die while not exposing the entire field. Because overlay error tends to be worse near the edges of the wafer, it is beneficial to have reference marks near the reference wafers' edge (*See* A New Approach to Correlating Overlay and Yield, *supra*). For the partially exposed field 3202 to be usefully included on the reference wafer, at least two completed or overlapped box-in-box structures should be present along the partially exposed fields' interlocking rows or columns. This facilitates determining the position of the partially exposed field relative to the other fields in the reference wafer.

Wafer Alignment Mark Exposures

Next the reference reticle containing the wafer alignment marks, as shown in Figure 13B, is loaded into the exposure position on the machine. The wafer alignment marks are exposed in openings in the previously defined Nfx X Nfy field array and placed so that it's interlocking rows and columns interlock or overlap the interlocking rows and columns already placed with the previous reference reticle. The result is schematically shown in Figure 16A where two wafer alignment marks 1604 suitable for a 0 degree wafer orientation

have been printed. The left wafer alignment mark (Figure 16A, field i=1, j=4) overlaps the previously placed reference reticle array along its' top and bottom interlocking rows and along its' right interlocking column while the right wafer alignment mark (Figure 16A, field i=7, j=4) overlaps the previously placed reference reticle array along its' top and bottom interlocking rows and along it's left interlocking column. Additional (optional) wafer alignment marks 1608 suitable for a 90 degree wafer orientation and interlocked into the field pattern are also shown.

Develop, Etch, Strip

After the last exposure is complete, the wafer is removed from the wafer stage and sent through the final resist development steps. Next, the alignment attributes and wafer alignment marks for each reference wafer are permanently etched into the reference wafer using a standard semiconductor etch process. The remaining resist is then stripped. An additional overcoating (SiO2 overcoating, for chrome over quartz) is possibly provided. Figures 35A-35F show a variety of vertical cross sections for the resulting reference mark (in this instance an inner box). The dashed vertical lines are the silicon wafer (or other substrate) while the diagonal lines represent a pre or post exposure deposited or overcoated layer. Thus in the case of a silicon wafer provided before exposure with a silicon dioxide, polysilicon, amorphous silicon, or silicon nitride coating, the reference marks would have the cross section of Figure 35C. Other vertical structures are clearly possible.

Measure Interlocking Rows And Columns

Referring to block 610 of Figure 6, at this point, the interlocking array row and column overlay target positions are measured. That is, the overlay errors present in the completed alignment attributes (box in box structures) present along the interlocking rows and columns (Figure 12 in detail and Figure 16A schematically) of the reference wafer are measured. In general, at least two distinct box-in-box overlay targets should be measured along each edge (top, bottom interlocking row and left, right interlocking column) of the interior fields. Referring to Figure 16A, a field (i,j) is an interior field if all of its' neighboring fields interlocking rows and columns are completely present on the wafer. For other fields, typically, at least 2 distinct measurements altogether distributed amongst its' interlocking rows and columns. in the overlapping regions. Increasing the number of

measurements along the interlocking rows and columns is desirable because this may increase the accuracy of the resulting calibration file, as shown in Figure 34, that characterizes the reference wafer. The aforementioned alignment attributes or box-in-box along the interlocking rows and columns are then measured an overlay metrology tool such as a KLA-Tencor model 5105 or 5200 (*See* KLA 5105 Overlay Brochure, *supra*; KLA 5200 Overlay Brochure, *supra*) or a Bio-Rad Semiconductor Systems Quaestor Q7. *See* Quaestor Q7 Brochures, *supra*. The resulting overlay data set is saved and entered into a computer algorithm for analysis and the overlay positional coordinates of the alignment attributes are computed and then saved for the subsequent calculation of the calibration file.

Intra-Field Distortion

Referring to block 612 of Figure 6, the intra-field or within the exposure field distortion pattern of the machine being used to create the reference wafer is provided. This can come from a variety of sources since a number of techniques are available for the determination of the intra-field distortion (dxf, dyf). One technique is described by Smith, McArthur, and Hunter, "Method And Apparatus For Self-Referenced Projection Lens Distortion Mapping", U.S. provisional application serial No. 60/254,271 filed December 8, 2000 and U.S. patent application serial No. 09/835,201 of the same title filed April 13, 2001. These patent applications describe a self referencing technique that can be carried out using overlay metrology tools widely available in semiconductor factories and allows for highly accurate determination of the intra-field distortion (dxf, dyf) over a set of grid points to within an x, y translation, rotation, and overall scale or symmetric magnification factor. Another technique is to expose on a photoresist coated wafer, a reticle pattern containing simple crosses or squares as illustrated in Figure 24 that are located at the desired intra-field grid positions illustrated in Figure 31. The wafer is then developed and the position of the resulting grid of boxes is measured using an absolute metrology tool such as a Leica LMS2000, Leica IPRO (Leica Microsystem, Wetzlar, Germany, (*See* Leica LMS IPRO Brochure, Leica), Nikon 51 or Nikon 61 (Nikon, Tokyo, Japan, (*See* Measuring System XY-5I, K. Kodama et al., SPIE Vol. 2439, 144:155, 1995)).

The technique described above is highly accurate but absolute metrology tools are not widely available in semiconductor factories and so it typically is not used. Yet another

technique involves assuming that the machines' inter-field or stage errors are small over the dimensions occupied by a single field, then printing a small field where a single inner box on a reticle is stepped around by the wafer stage to a grid of locations in the field. Then another reticle containing an array of complementary outer boxes covering the full image field is printed over the inner boxes and the resulting box in box measurements are directly interpreted as the intra-field distortion. *See* A "Golden Standard" Wafer Design for Optical Stepper Characterization, *supra*. This technique is the least accurate and least preferred. With all of these techniques, the overall scale or symmetric magnification is determined with a greater or lesser degree of accuracy, more on this below.

Calculate Calibration File

Referring to block 614 of Figure 6, the reference wafer calibration file calculated. This is the step that creates a unique calibration file for each reference wafer. Because the intra-field errors are known, they can be combined with the overlay measurements made along the interlocking rows and columns of the reference wafer to determine the stage or inter-field errors. Then combining the determined stage errors with the intra-field errors produces the calibration file that contains the locations of all of the reference marks on a wafer scale periodic grid (P/M = period) and the positions of the wafer alignment marks. The step of determining the inter-field errors uses the techniques described in Smith, McArthur, and Hunter ("Method And Apparatus For Self-Referenced Positional Error Mapping", U.S. provisional application serial No. 60/254,413 filed December 8, 2000 and U.S. patent application serial No. 09/891,699 of the same title filed June 26, 2001).

The following model may be used in the determination of the stage errors:

$$\begin{aligned} BBx(i,j;a,T) &= [dxG(i,j+l) + dxf(a,B) - Qg(ij+l)*yfn(B)] - [dxG(i,j) + dxf(a,T) - Qg(i,j)*yfn(T)] \\ &= dxG(i,j+l) - dxG(i,j) - Qg(ij+l)*yfn(B) + Qg(i,j)*yfn(T) + dxf(a,B) - dxf(a,T) \end{aligned} \quad \text{(Eq 4)}$$

$$BBy(i,j;a,T) = [dyG(i,j+l) + dyf(a,B) + Qg(i,j+l)*xfn(a)] - [dyG(i,j) + dyf(a,T) + Qg(ij)*xfn(a)]$$

$$= dyG(i,j+1) - dyG(i,j) + Qg(i,j+1)* xfn(a)- Qg(i,j)*xfn(a) + dyf(a,B) - dyf(a,T) \quad \text{(Eq 5)}$$

$$BBx(i,j;b,R) = [dxG(i+1,j) + dxf(b,L) - Qg(i+1,j)*yfn(b)] - [dxG(i,j) + dxf(b,R) - Qg(i,j)*yfn(b)]dxG(i+1,j) - dxG(i,j) - Qg(i+1,j)*yfn(b) + Qg(i,j)*yfn(b) + dxf(b,L) - dxf(b,R) \quad \text{(Eq 6)}$$

$$BBy(i,j;b,R) = [dyG(i+1,j) + dyf(b,L) + Qg(i+1,j)*xfn(L)] - [dyG(i,j) + dyf(b,R) + Qg(i,j)*xfn(R)] dyG(i+1,j) - dyG(i,j) + Qg(i+1,j)*xfn(L) - Qg(i,j)*xfn(R) + dyf(b,L) - dyf(b,R) \quad \text{(Eq 7)}$$

Where:

T, B, R, L = designate the top, bottom, right and left most row or column within each field [see Figure 31].

(i, j) = field indices [see Figures 17A and 31]. i=1:Nfx, j=1:Nfy but not all i, j pairs occur Equations 4-7. If the field or the corresponding measurement set (T or R) does not occur then that equation is absent. That is, i labels fields consecutively left to right while j labels fields consecutively from bottom to top.

(a, b) = intra-field indices or indices corresponding to each feature [Figure 31], a=1:Nx+2, b=1:Ny+2. That is, a labels features consecutively left to right while b labels features consecutively from bottom to top.

xf(L), xf(R) = x intrafield nominal position of left (a=1) , right (a=Nx+2) interlocking columns [Figures 15 and 31]. These are known quantities.

yf(T), yf(B) = y intrafield nominal position of the top (b=Ny+2), bottom (b=1) interlocking rows [Figures 15 and 31]. These are known quantities.

xfn(a), yfn(b) = (x,y) intrafield nominal position of feature with index (a,b). These are known quantities (see Figure 15 for relative positions on the reticle);

BBx, BBy(i,j;a,T) = (x,y) measured overlay errors along the top (b=Ny+2) interlocking row of field (i,j) at column a. Thus, "a" covers the range a=2:Nx+1 but the actual number of measurements made along this edge is at the user's discretion subject to the

availability of a site on partially exposed fields. See above for the number of measurements required for the purposes of this invention. These are known quantities.

BBx, BBy(i,j;b,R) = (x,y) measured overlay errors along the right (a=Nx+2) edge of field (i,j) at row b. "b" covers the range b=2:Ny+1 but the actual number of measurements made along this edge is at the user's discretion subject to the availability of a site on partially exposed fields. These are known quantities.

dxG(i,j), dyG(i,j), Qg(i,j) = inter-field placement errors in x, y, and yaw or rotation at field (i,j). These are the error terms that characterize the wafer stage stepping. These quantities are solved for, to construct the calibration file.

dxf(b,L), dyf(b,L) = x,y intra-field lens distortions along the left interlocking column (a=l) of the field [Figure 31]. These are known quantities.

dxf(b,R), dyf(b,R) = x,y intra-field lens distortions along the right interlocking column (a=Nx+2) of the field [Figure 31]. These are known quantities.

dxf(a,T), dyf(a,T) = x,y intra-field lens distortions along the top interlocking row (b=Ny+2) of the field [Figure 31]. These are known quantities.

dxf(a,B), dyf(a,B) = x,y intra-field lens distortions along the bottom interlocking row (b=1) of the field [Figure 31]. These are known quantities.

Thus, all of the quantities in Equations 4-7 are known except the inter-field or grid error (dxG, dyG, Qg)(i,j) which must be solved for. Equations 4-7 are typically over determined in the sense of equation counting (there are more equations than unknowns) but are still singular in the mathematical sense; the null space of Equations 4-7 has a dimension of three. *See* Numerical Recipes, The Art of Scientific Computing, W. Press et al., Cambridge University Press, 52:64, 1990. Now it can be mathematically shown that this 3-dimensional null space corresponds to our inability to uniquely solve for the inter-field error to within an overall X or Y translation and an overall rotation. Put differently, if error (dxG, dyG, Qg)(i,j)) is a solution to Equations 4-7, then (dxG(i,j) + Tx - qg*yG(i,j) , dyG(i,j) + Ty + qg*xG(i,j), Qg(i,j) + qg) is also a solution of Equations 4-7 where:

Tx, Ty = arbitrary translation,

qg = arbitrary rotation

(xG,yG)(i,j) is the nominal center position in wafer coordinates of field (i, j).

To uniquely define a solution we can require that the computed solution have zero values for these modes. Then:

$$\Sigma\, dxG(i,j) = 0 \quad \text{no x translation} \qquad \text{(Eq 8)}$$

$$\Sigma\, dyG(i,j) = 0 \quad \text{no y translation} \qquad \text{(Eq 9)}$$

$$\Sigma\, yG(i,j)*dxG(i,j) - xG(i,j)*dyG(i,j) = 0 \quad \text{no rotation} \qquad \text{(Eq 10)}$$

Σ denotes summation over all inter-field grid point pairs (i, j) whose offsets and yaws are to be determined. Equations 4-7 are typically solved using the singular value decomposition to produce the minimum length solution. *See* Numerical Recipes, The Art of Scientific Computing, *supra*. It can be shown that the constraints of Equations 8-10 effectively define a unique solution within the null space of Equations 4-7, and therefore they can be applied after the minimum length solution (dxGm, dyGm, Qg)(i,j) has been determined.

Using Eq 11-13 below we solve for Tx, Ty, qg:

$$\Sigma\, dxGm(i,j) + Tx - qg*yG(i,j) = 0 \qquad \text{(Eq 11)}$$

$$\Sigma\, dyGm(i,j) + Ty + qg*xG(i,j) = 0 \qquad \text{(Eq 12)}$$

$$\Sigma\, yG(i,j)*(dxGm(i,j) + Tx - qg*yG(i,j)) - xG(i,j)*(dyGm(i,j) + Ty + qg*xG(i,j)) = 0 \qquad \text{(Eq 13)}$$

and the inter-field distortion array satisfying Eq 8-10 and Eq 4-7 is:

$$dxG(i,j) = dxGm(i,j) + Tx - qg*yG(i,j) \qquad \text{(Eq 14)}$$

$$dyG(i,j) = dyGm(i,j) + Ty + qg*xG(i,j) \qquad \text{(Eq 15)}$$

$$Qg(i,j) = Qgm(i,j) + qg \qquad \text{(Eq 16).}$$

At this point, having uniquely determined the inter-field distortion array, we can calculate the reference wafer calibration file. At a minimum, the following four quantities

(xG, yG, dx, dy) are recorded into the wafer calibration file for each feature in the reference array which is on regular pitch P/M and each wafer alignment mark:

(xG, yG) = nominal (x,y) position of feature on the wafer (interfield or grid coordinates with center of coordinate system at wafer center (x,y axes in Figure 33)),

(dx, dy) = offset or error in nominal position of feature on the wafer. The true position of the feature is given by:

(Xtrue, Ytrue) = (xG + dx, yG + dy) = true position of feature on wafer. (Eq 17)

The nominal positions (xG, yG) of all features on the wafer are known to us because they are the positions as they would be placed by a perfect projection imaging system using perfect reference reticles. These numbers are known since both the stepping pattern on the reference wafer is known as well as the design of the reference reticles.

The offset errors of a feature located at intra-field index (a,b) within exposure field (i,j) on the reference wafer the offset error (dx, dy) is calculated as:

$$dx(a,b;i,j) = dxG(i,j) - Qg(i,j)*xf(a) + dxf(a,b) \quad \text{(Eq 18)}$$

$$dy(a,b;i,j) = dyG(i,j) + Qg(i,j)*yf(b) + dyf(a,b). \quad \text{(Eq 19)}$$

All of the quantities on the right hand side of Eq. 18 and 19 are known and therefore (dx, dy) is directly determined. This suffices for the determination of the offset errors for the reference array on regular pitch P/M (Figure 33).

For wafer alignment marks, WM, that cover a more extended region or off grid portion of projection field (i,j) we would use the following formulas to determine the offset error:

$$dx(WM,i,j) = dxG(i,j) - Qg(i,j) * \langle xf \rangle(WM) + \langle dxf \rangle(WM) \quad \text{(Eq 20)}$$

$$dy(WM,i,j) = dxG(i,j) + Qg(ij) * \langle yf \rangle(WM) + \langle dyf \rangle(WM) \quad \text{(Eq 21)}$$

where:

(<xf~>, <yf>)(WM) = (x,y) center of mass or average position of WM in intra-field coordinates, and

(<dxf>, <dyf>)(WM) = average intra-field distortion of WM. This is calculated by interpolating the given values for intra-field distortion, (dxf, dyf)(a,b), so that they apply everywhere in the field and then calculating the area weighted offset of all of the components making WM. Having computed all of the nominal positions and offsets we create a file (Figure 34) detailing the feature, xG, yG, dx, dy, and possibly other information. This file is uniquely associated with a particular reference wafer (Figure 33).

Final Articles

The final articles that result from the process of Figure 6 is a completed reference wafer (Figure 33) and corresponding calibration file (Figure 34). Because the reference wafer of Figure 33 has a wafer scale (covering the entire wafer, not limited to a single exposure field) reference array (pitch = P/M) that is uninterrupted by field boundaries, and the position of each reference mark and wafer alignment mark is accurately known from the calibration file and Eq 17, the article can be used to perform stepper and scanner matching without any regard to field size or format. *See* System and Method for Optimizing the Grid and Intrafield Registration of Wafer Patterns, *supra*; Mix-and-Match: A Necessary Choice, *supra*; Expanding Capabilities in Existing Fabs with Lithography Tool-Matching, *supra*. Thus, the interlocking rows and columns of the reference wafer that were vital to the accurate determination of position, though they physically remain, are not a concern and do not interfere with users of the reference wafer; all that is required is the reference wafer and its' calibration file.

Alternate Embodiment

Similar process steps as described above are used except for being adapted to step and scan tools (scanners) (*See* Optical Lithography – Thirty Years and Three Orders of Magnitude, *supra*) by exposing the wafer alignment marks and the interlocking reference arrays with multiple sub-Eo exposures, and also providing a reticle with reduced transmission. Eo (E-zero) is the minimum exposure dose required for a large (> 200 micron at wafer) open area pattern on the reticle to become fully developed or cleared (in the case of positive resist). Eo depends on the particular resist and resist development process. The

intra-field error of scanners has an intrinsic non-repeatable component (0.7 NA DUV Step and Scan System for 150nm Imaging with Improved Overlay, *supra*) whose effect on the manufactured reference wafers is desired to minimize. Reference reticles, similar to the reticles shown in Figures 13A and 13B, may be provided with a partially reflecting dielectric coating either on their non-chrome or possibly chrome coated (machine optical object plane) surface as shown in Figure 14. For example, a 95% reflecting dielectric coating applied to the reference reticles means that if twenty exposure sequences at a dose of 2*Eo each are performed the net effect is to expose the wafer with a dose of 2*Eo and to have effectively averaged over as many as twenty exposures. An advantage of this technique is that it averages out the non-repeatable part of the scanner error. Thus, if the reference wafer requires a dose of b*Eo, and we expose at a dose of a*Eo, the overlay reticle has a coating that reflects a fraction R of light incident on it, then the number of exposures (N) required to get a dose of b*Eo on the reference wafer is:

$$N = 1 + \text{floor}(b/(a*(I-R)) \qquad \text{(Eq 22)}$$

and

floor(x) = integer part of the real number x.

As a typical example, exposing at a dose of 1*Eo (a=l), using reference reticles that are 90% reflecting (R=0.90) and requiring a dose on the reference wafers of 2*Eo (b=2) means the number of required exposures is (Eq 22) N=21 resulting in effectively averaging over as many as twenty-one realizations of the intra-field distortion. While this embodiment has been described with respect to a partially reflecting reticle, there are similar considerations if the overlay reticle is absorbing or attenuated. An attenuated phase shift mask is well suited for this purpose (*See* The Attenuated Phase Shift Mask, B. Lin) instead of reflecting; all that is required is a reticle with a decreased optical transmission from normal. In general, the reticle typically needs an optical transmission (1-R for a reflective mechanism) of < 50% of normal or nominal.

Reference Reticle Fabrication

The reticle plate, as shown in Figures 13A, 13B and 14, makes no requirements on the size of the reticle plate, the design of the overlay targets or alignment attributes or the types of materials used to fabricate it. In cases where it might be necessary to have more wafer alignment marks a third or multiple reference reticles might be appropriate. Alternatively, both the interlocking array with reference marks and the wafer alignment marks could be contained on one and the same reticle. This is especially practical if the reference wafers are to be manufactured on a scanner using the scanner's static field, then there is certainly room on a single reticle for both. Heretofore, we have considered the reticle creating the patterns as perfect. In practice it is, not but errors in the reticle manufacture can be taken into account by first measuring the position of all the individual structures on the reference reticle using an absolute metrology tool such as the Nikon 51 (*See* Measuring System XY-5I, *supra*), or Leica IPRO series tools. *See* Leica LMS IPRO Brochure, *supra*. Next, in formulating Equations 4-7, this reticle error (divided by the projection imaging tool demagnification (M)) is explicitly written out on the right hand side and then subtracted from the resulting overlay measurements on the left hand side of the equations (thereby canceling out on the right hand side). The result is Equations 4-7 as they are written above but with a correction applied to the overlay measurements appearing on the left hand side. This accounts for the reticle error in the determination of the inter field grid and yaw distortion (dxG, dyG, Qg). The other correction for reticle distortion is directly added to the dx or dy term of Equations 18-21 as the reference reticle error at the feature we are considering divided by M.

Additional Embodiments

Thus far, embodiments have been mainly described with respect to alignment attributes that are in the form of a box in box or frame in frame pattern as shown in Figure 11A. Other alignment attributes such as gratings (*See* Overlay Alignment Measurement of Wafers, *supra* [Fig 1b], wafer alignment marks (*See* Matching Management of Multiple Wafer Steppers Using a Stable standard and a Matching Simulator, *supra*), van der Pauw resistors (*See* Automated Electrical Measurements of Registration Errors in Step and Repeat Optical Lithography Systems, *supra*), vernier pairs (*See* Method of Measuring Bias and Edge

Overlay Error for Sub 0.5 Micron Ground Rules, *supra*), or capacitor structures (*See* Capacitor Circuit Structure for Determining Overlay Error, *supra*) could be used instead. In general, any alignment attribute that can be used by an overlay metrology tool for measuring offsets can be utilized.

The overlay metrology tool utilized is typically a conventional optical overlay tool such as those manufactured by KLA-Tencor (*See* KLA 5105 Overlay Brochure, *supra*; KLA 5200 Overlay Brochure, *supra*) or Bio-Rad Semiconductor Systems. *See* Quaestor Q7 Brochures, *supra*. Other optical overlay tools can also be used. *See* Process for Measuring Overlay Misregistration During Semiconductor Wafer Fabrication, *supra* or *See* Overlay Alignment Measurement of Wafers, *supra*. In addition, some steppers or scanners can utilize their wafer alignment systems and wafer stages to function as overlay tools (*See* Matching Management of Multiple Wafer Steppers Using a Stable standard and a Matching Simulator, *supra*). In general, the total size of the alignment attribute is limited (in this case consisting of two wafer alignment marks) to a distance over which the wafer stage would be as accurate as a conventional optical overlay tool. This distance is typically < 0.5 mm. When electrical alignment attributes are used for overlay (*See* Electrical Methods for Precision Stepper Column Optimization, L. Zych et al., SPIE Vol. 633, 98:105, 1986; Automated Electrical Measurements of Registration Errors in Step and Repeat Optical Lithography Systems, *supra*, Capacitor Circuit Structure for Determining Overlay Error, *supra*), the overlay metrology tool would correspond to the electrical equipment utilized for making the corresponding measurement.

Thus far, the description has been with respect to manufacture and use of a reference wafer on the projection imaging tools (steppers (*See* Direct-Referencing Automatic Two-Points Reticle-to-Wafer Alignment Using a Projection Column Servo System, *supra*; New 0.54 Aperture I-Line Wafer Stepper with Field by Field Leveling Combined with Global Alignment, *supra*; Projection Optical System for Use in Precise Copy, T. Sato et al., U.S. Patent 4,861,148 issued August 29, 1989), and scanners (*See* Micrascan™ III Performance of a Third Generation, Catadioptric Step and Scan Lithographic Tool, *supra*; Step and Scan Exposure System for 0.15 Micron and 0.13 Micron Technology Node, *supra*; 0.7 NA DUV Step and Scan System for 150nm Imaging with Improved Overlay, *supra*) most commonly

used in semiconductor manufacturing today. However, the articles described can be manufactured or applied to other projection imaging tools such as contact or proximity printers (*See* Optical Lithography – Thirty Years and Three Orders of Magnitude, *supra*), 2-dimensional scanners (*See* Large Area Fine Line Patterning by Scanning Projection Lithography, *supra*; Large-Area, High-Throughput, High-Resolution Projection Imaging System, *supra*; Optical Lithography – Thirty Years and Three Orders of Magnitude, *supra*), office copy machines, and next generation lithography (ngl) systems such as XUV (*See* Development of XUV Projection Lithography at 60-80 nm, *supra*), SCALPEL, EUV (Extreme Ultra Violet) (*See* Reduction Imaging at 14nm Using Multilayer-Coated Optics: Printing of Features Smaller than 0.1 Micron, J. Bjorkholm et al., Journal Vacuum Science and Technology, B 8(6), 1509:1513, Nov/Dec 1990), IPL (Ion Projection Lithography), and EPL (electron projection lithography). *See* Mix-and-Match: A Necessary Choice, *supra*.

The above description utilized only a single projected wafer alignment mark. However, multiple types of wafer alignment marks, one for each type of tool in the fab we will be analyzing or different angular orientations, *See* Figure 33, could be projected to increase the utility of the reference wafer. In the case of multiple wafer alignment marks, the procedure would be modified so that the resulting calibration file would contain the nominal and offset position of all of the projected alignment marks.

While the above described laying down a series of reference marks on a regular, wafer scale array of pitch P/M. Any other pattern that is built up by interlocking fields along rows and columns can also be used. The positions of the resulting features can be measured and recorded in a calibration file that is determined as described above. In particular, a wafer could be created that consisted entirely of wafer alignment marks at precisely known positions as illustrated in Figure 36. Such a reference wafer and its' associated calibration file is valuable for assessing projection imaging tool alignment system performance.

The reference reticle is typically glass with openings defined in a chrome coating. This is common for projection lithography tools utilized in semiconductor manufacture. The form the reticle can take will be determined by the format required by the specific projection imaging tool on which the reticle is loaded. Thus, an extreme ultra-violet (XUV) projection

system would typically have a reflective reticle. *See* Development of XUV Projection Lithography at 60-80 nm, *supra*.

The embodiments described above have been mainly described with respect to the recording medium being positive photoresist. Negative photoresist could equally well have used providing appropriate adjustment to the box in box structures on the reticle are made. Other types of recording medium can also be used, for example, an electronic CCD, a diode array, liquid crystal, or other optically sensitive material. In general, the recording medium is whatever is typically used on the projection imaging tool used for manufacturing the reference wafers. Thus, on an EPL tool, an electron beam resist such as PMMA could be utilized as the recording medium.

So far, the substrates on which the recording media is placed have been described as wafers. This will typically be the case in semiconductor manufacture. The exact form of the substrate will be dictated by the projection imaging tool used for its' manufacture and it's use in a specific manufacturing environment. Thus, in a flat panel manufacturing facility, the reference substrate would be a glass plate or panel. Circuit boards or multi-chip module carriers are other possible substrates.

Figure 7 is a flow chart illustrating another embodiment for creating a reference wafer. In block 702 a reference reticle with reduced transmission is loaded into an exposure tools' reticle management system. Flow continues to block 704 where the wafer is then coated with photoresist and loaded into a projection imaging tool or machine. In block 706 the wafer is exposed, in an overlapping interlocking pattern, with multiple sub-E_0 exposures.

Flow then continues to block 708 where, after the final exposure the wafer is removed from the machine and sent through the final few resist development steps. Next, the wafers are etched and stripped of photoresist and possibly overcoated with another layer. This leaves the alignment attributes and wafer alignment marks permanently recorded on the wafer surfaces. Flow then continues to block 710 where the resulting alignment attributes along the interlocking rows and columns are measured for registration, placement or overlay error.

Next, in block 712, the intra-field distortion of the projection imaging tool used to create the reference wafer is provided. Flow continues to block 714 when the resulting data

set is entered into a computer algorithm where a special calibration file containing the positional coordinates for each alignment attribute is constructed for the reference wafer.

Figure 8 is a flow diagram of an example of an application of the reference wafer. Flow begins in block 802 and the reference wafer is loaded onto a machine. Flow continues to block 804 where an overlay reticle is loaded and aligned on the machine. Then in block 806 the reference wafer is exposed. In block 810 the wafer is developed and the overlay targets are measured. In block 812 the references wafer calibration file offsets are subtracted from the measurements. Then, in block 814 the inter-field or intra-field errors for the new machine are calculated.

The machine on which the reference wafer is loaded may be different types of imaging tools. For example, the machine may be a stepper projection imaging tool, a scanner projection imaging tool, an electron beam imaging system, an electron beam direct write system, a SCAPEL tool, an extreme ultra-violet imaging apparatus, an ion projection lithography tool, or an x-ray imaging system. Also, the subtraction of the calibration file and the calculation of the inter-field or intra-field errors may be performed on a computer or a controller. In addition, the calibration file may be stored on a computer readable medium, for example, a tape, a diskette, or a CD.

The foregoing description details certain embodiments of the invention. It will be appreciated, however, that no matter how detailed the foregoing appears, the invention may be embodied in other specific forms without departing from its spirit or essential characteristics. The described embodiments are to be considered in all respects only as illustrative and not restrictive and the scope of the invention is, therefore, indicated by the appended claims rather than by the foregoing description. All changes which come with the meaning and range of equivalency of the claims are to be embraced within their scope.